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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Ex parte TUYET-HUONG THI NGUYEN, GEORGE MATHEW, WAI-MING RICHARD CHAN, and MUKUND P. KHATRI

Appeal 2008-4163
Application 09/768,665
Technology Center 2100

Decided:[1] April 29, 2009

Before JOSEPH L. DIXON, JEAN R. HOMERE, and JAY P. LUCAS, *Administrative Patent Judges*.

DIXON, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

I. STATEMENT OF THE CASE

A Patent Examiner rejected claims 1, 4-8, 16, and 19-23. The Appellants appeal therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b). We AFFIRM.

INVENTION

The invention at issue on appeal relates to a method for managing software system management interrupt (hereinafter SMI) in a multiprocessor computer system. (Spec. 1.)

ILLUSTRATIVE CLAIM

Claim 22, which further illustrates the invention, follows.

> 22. A method for handling a system management interrupt in a multiprocessor computer system, wherein each of the multiple processors of the computer system is capable of operating as a system management interrupt handler and wherein none of the processors are dedicated to processing the system management interrupt of the computer system, comprising the steps of:
>
> receiving at each of the processors an instruction to enter a mode associated with the issuance of a system management interrupt;
>
> selecting a designated processor from among the set of processors capable of operating as a system management interrupt handler, as a system management interrupt handler,

the selection of the designated processor being accomplished according to an arbitration scheme;

scanning the memory location containing saved contents of each processor of the computer system;

locating in the memory location a signature identifying the saved contents of the processor that issued an instruction that caused the system management interrupt; and

retrieving from the saved contents of the issuing processor parameters necessary for handling of the system management interrupt.

REFERENCES

The Examiner relies on the following references as evidence:

Smith	3,643,227	Feb. 15, 1972
Goodman	6,282,601 B1	Aug. 28, 2001 (filed Mar. 13, 1999)
Appellants' Admitted Prior Art ("AAPA")		(Spec. 2, l. 3- 3, l. 21)

REJECTION

The Examiner rejects the claims in this appeal as follows:

Claims 1, 4-8, 16, and 19-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Goodman and Smith.

We note that Appellants have identified independent claims 1, 14, and 16, but independent claims 1, 16, and 22 are pending and under review. (App. Br. 5). Since Appellants have not separately argued each of the independent claims, and Appellants' arguments have treated all independent

claims as a single group which stand or fall together, we select claim 22 as the representative claim for this group. *See* 37 C.F.R. § 41.37(c)(1)(vii).

II. ISSUES

Based upon our review of the administrative record, we have determined that the following issues are dispositive in this appeal:

Have Appellants shown that the Examiner erred in finding that the proffered combination of references fails to teach or fairly suggest a plurality of computer processors, wherein each of said processors is capable of operating as a system management interrupt handler and wherein none of the processors is dedicated to processing system management interrupt of the computer system, are recited in the preamble of independent claim 22? (App. Br. 8, Reply Br. 5).

Have Appellants shown that the Examiner erred in combining the teachings of Goodman with the other references? (App. Br. 6-8, Reply Br. 5-6). The issue further turns on whether the teachings of Goodman such as utilizing a dedicated processor as the system interrupt handling processor teaches away from the claimed invention.

III. PRINCIPLES OF LAW

Prima Facie Case of Unpatentability

The allocation of burdens requires that the USPTO produce the factual basis for its rejection of an application under 35 U.S.C. §§ 102 and 103. *In re Piasecki*, 745 F.2d 1468, 1472 (Fed. Cir. 1984) (citing *In re Warner*, 379 F.2d 1011, 1016 (CCPA 1967)). The one who bears the initial burden of presenting a prima facie case of unpatentability is the Examiner. *In re*

Oetiker, 977 F.2d 1443, 1445 (Fed. Cir. 1992). Appellants have the opportunity on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006).

Claim Interpretation

During prosecution before the USPTO, claims are to be given their broadest reasonable interpretation, and the scope of a claim cannot be narrowed by reading disclosed limitations into the claim. *See In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997).

"Giving claims their broadest reasonable construction 'serves the public interest by reducing the possibility that claims, finally allowed, will be given broader scope than is justified.'" *In re American Academy of Science Tech Center*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (quoting *In re Yamamoto*, 740 F.2d 1569, 1571 (Fed. Cir. 1984)). "Construing claims broadly during prosecution is not unfair to the applicant . . . because the applicant has the opportunity to amend the claims to obtain more precise claim coverage." *Id.,* at 1364.

A preamble is construed as a limitation "if it recites essential structure or steps, or if it is 'necessary to give life, meaning, and vitality' to the claim." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (quoting *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999)). A preamble is not limiting, however, "'where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.'" *Id.* (quoting *Rowe v. Dror*, 112 F.3d 473, 478 (Fed. Cir. 1997)).

35 U.S.C. § 103(a)

In rejecting claims under 35 U.S.C. § 103, "[w]hat matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under § 103." *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 419 (2007). To be nonobvious, an improvement must be "more than the predictable use of prior art elements according to their established functions." *Id.* at 417.

IV. FINDINGS OF FACT

In our analysis *infra*, we will rely on the following findings of fact (FF) that are supported by a preponderance of the evidence:

1. Appellants filed an amendment, with the second Request for Continued Examination (hereinafter RCE) on Mar. 9, 2006, which contains the added limitations "wherein none of the processors are (sic) dedicated to processing the system management interrupts of the computer system."

2. Goodman discloses a system and method for handling SMI within a multi-processor computer system. One of the processors (boot processor 12a) worked with an interrupt hardware (60) is dedicated to handle SMI. The boot processor scans the saved content in SMI request register (62) and retrieves the saved contents to determine which processor requests the interrupt and what type of SMI service is requested. (Col. 2 ll. 8-25 and Col. 5 ll. 15-62, Figs. 1 and 4). Goodman does not expressly or impliedly disclose prohibiting, criticizing, discrediting or otherwise discouraging the scanning scheme being utilized in a multi-processor computer system wherein none of the processors is dedicated to handle SMIs.

3. AAPA teaches that in a multiprocessor computer system, each of the processors having its own SMI handler will enter system management mode and save the contents in its register and the operating code used by its SMI handler to a storage space located to the processor upon receiving the SMI. A processor will be then selected from the processors to handle the SMI. (Spec. 2-3).

V. ANALYSIS

From our review of the Examiner's stated rejections, we find that the Examiner appears to have set forth a detailed explanation of the rejection. We find the Examiner's showing to set forth a *prima facie* case of obviousness. Therefore, we look to Appellants' Briefs to show error in the proffered *prima facie* case.

With respect to representative independent claim 22, Appellants contend that the prior art references as applied by the Examiner, "taken alone or in combination, do not teach or suggest all of the claim limitations of the present invention." In particular, Appellants contend that the Examiner failed to teach or suggest the language in the preamble of the claim 22, "each of the multiple processors of the computer system is capable of operating as a system management interrupt handler and wherein none of the processors are (sic) dedicated to processing system management interrupts of the computer system" (App. Br. 8, Reply Br. 5).

The Examiner states that "Goodman is relied upon in the above 103 Rejection … Goodman discloses scanning the contents of the memory space associated with each processor" (Ans. 11) and the Examiner previously stated that "the acknowledged prior art further discloses that a different

processor, other than the processor initiating the interrupt, may be selected for handling the interrupt." (Final Rejection 12).

At the outset, we note that neither Appellants nor the Examiner expressly discussed the scope of the argued limitations present in the preamble of the claims under review. Thus, we start our review by first determining the appropriate scope of representative claim 22.

We note that Appellants' claim 22 (and other independent claims in the amendment filed with the second RCE filing) was amended by adding the express language of "none of the processors are dedicated to processing system management interrupt" (hereinafter "limitation 1") into the preamble of claim 22. (FF 1). Thus, the preamble of claim 22 has two limitations, one is the limitation 1 and the other is "each of the multiple processors of the computer system is capable of operating as a system management interrupt handler of the computer system" (hereinafter "limitation 2"). When the body of the claim following the preamble is a self-contained description of the structure and does not depend on the preamble for completeness, the preamble does not usually limit the claim. *IMS Technology Inc. v. Hass Automation Inc.* 54 USPQ2d 1129, 1137 (Fed. Cir. 2000).

We note that the body of claim 22 does not recite limitation 1 or reference this limitation. We further note from the file history that the purpose of adding the limitation 1 into the independent claims by Appellants was an attempt to exclude the Goodman reference because Goodman teaches utilizing a dedicated processor to handle SMI. We find that body of the claim 22, while given a broad yet reasonable interpretation, is a self-contained description of a complete process to select one processor to handle SMIs, to scan the memory location containing saved contents of each

processor of the computer system, to locate in the memory location a signature identifying the saved contents of the processor, and to retrieve from the saved contents of the issuing processor information for handling the interrupt. Thus, the body of claim 22 does not depend on limitation 1 of the preamble for completeness. Nor does limitation 1 recite essential structure or steps, nor is it "necessary to give life, meaning, and vitality" to the claim. Hence, we conclude that limitation 1 in the preamble does not limit claim 22.

We next look at the limitation 2 of the preamble. If the body of a claim fully and intrinsically sets forth all of the limitations of the claimed invention, and the preamble merely states, for example, the purpose or intended use of the invention, rather than any distinct definition of any of the claimed invention's limitations, then the preamble is not considered a limitation and is of no significance to claim construction. *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999). Here, the body of claim 22 does not recite limitation 2 and does not depend on limitation 2 of the preamble for completeness. Further, limitation 2 in the preamble of claim 22 merely sets forth the multiprocessor computer environment where the interrupt takes place by stating that each multiprocessor is capable of handling the SMIs. Hence, we conclude that limitation 2 in the preamble does not limit claim 22.

Therefore, we find both limitations in the preamble of claim 22 are not entitled to patentable weight since they are limited only in the preamble, and they do not breathe life into the body of the claim 22. We find the body of claim 22 is a self-contained description and structurally complete invention.

We now address the merits of the contentions of Appellants. Since the preamble of claim 22 is not entitled to patentable weight from our claim construction, we find that Appellants' contentions regarding the preamble are not persuasive of error in the Examiner's showing of a prima facie case of obviousness. Hence, Appellants have failed to show that the Examiner erred in finding that the prior art combination teaches or fairly suggests the limitations in the preamble of claim 22.

In the interest of completeness, we will also consider whether the Examiner's reliance on AAPA is misplaced. Assuming that the preamble of representative claim 22 were given patentable weight and thereby be construed as including each of the processors is capable of processing the system management interrupt and none of them is being dedicated to process the interrupt, we would still agree with the Examiner's rationale that AAPA discloses that any one processor among the multiprocessor system can be selected to handle SMIs. Thus, none of the processors in the multiprocessor system would be a dedicated processor to handle SMIs. (Final Action, 12, FF3).

Appellants also contend that "the cited portions of the Background [sic, Summary of the Invention] of Appellants' Specification discuss how, in a multi-processor system, a second processor may be *unable* to properly process a system management interrupt." Thus, Appellants contend that the AAPA does not teach the limitations in the preamble of claim 22. (App. Br. 8-9, Reply Br. 5).

We disagree with Appellants. AAPA teaches that each processor has its own SMI handler. Thus, each processor of the multiprocessor computer system is capable of handling the SMI (FF3). We find that Appellants'

argument is not commensurate in scope with the express language "capable of" of the limitations since the scope of the limitations does not include that each processor must be able to handle SMI. Thus, we agree with the Examiner that AAPA discloses all limitations in the preamble of claim 22 (FF3). Therefore, Appellants have failed to show that the Examiner erred in finding that prior art teaches or fairly suggests the language in the preamble of claim 22.

We next address the issue whether Goodman teaches away from the claimed invention. Appellants further contend that Goodman cannot be combined with AAPA or any other reference because

> Goodman teaches away from the claimed invention by *expressly* providing that all system management interrupts are to be handled by a **single, dedicated** processor….There is no teaching from Goodman to suggest that *any* processor other than the single boot processor is operable to handle a system management interrupt. Nowhere does Goodman suggest that multiple processors could be used to handle system management interrupts, as explicitly claimed in the present application. A plain reading of Goodman would lead a person of ordinary skill to conclude that only a **single, dedicated** processor is responsible for handling a system management interrupt, in direct contrast to the claims of the present invention. Here, when considering the teachings of Goodman as a whole, a person of ordinary skill would be encouraged to use only a **single, dedicated** processor as the processor responsible for handling a system management interrupt. When considered as a whole, the prior art counsels *directly* against Appellants' invention. This is "strong evidence" of the nonobviousness of the invention because Goodman teaches a solution that is the *opposite* of the invention of the present application… Therefore, Appellants respectfully submit that Goodman must be considered in its entirety, and, when Goodman is considered in its entirety, Goodman teaches away from the claimed invention.

(App. Br. 7-8, Reply Br. 3-4).

We disagree with Appellants. It is our reasoned conclusion that Goodman is not a reference teaching away from the claimed invention even viewing Goodman in its entirety. Thus, Goodman should not be excluded from the obviousness rejection.

First, we do not find and Appellants have not identified any express or implied teachings in the disclosure of Goodman for criticizing, discrediting or otherwise discouraging the solution claimed (FF2).

Furthermore, we view Goodman's teaching of a dedicated processor for handling the SMI is simply one way to handle SMI in multi-processor computer system. Appellants did not present any evidence that Goodman's scanning scheme cannot be used in non-dedicated multi-processor environment.

Finally, contrary to Appellants' arguments concerning "teaching away," we find the Examiner's position to be reasonable that "the teaching of Goodman, not only beneficially used to solve the problem of severe interrupt timing constraint in a multi-processor system, wherein one processor is dedicated to interrupt processing, but also can be used in multi-processor system, wherein none of the processors is dedicated for interrupt processing (any processor can process interrupts)." (Ans. 12-13).

Therefore, we find Appellants' argument is unpersuasive that the Examiner erred in combining the teachings of Goodman with other references. Independent claims 1 and 16 contain similar limitations as in claim 22, and fall with representative independent claim 22.

Accordingly, we sustain the Examiner's § 103(a) rejection of claims 1, 16, and 22. Dependent claims 4-8, 19-21, and 23 fall with the base claims.

37 C.F.R. § 41.37(c)(1)(vii) (2007). *In re Nielson*, 816 F.2d 1567, 1572 (Fed. Cir. 1987).

VI. CONCLUSION

For the aforementioned reasons, we conclude that Appellants have not shown that the Examiner erred finding that the proffered combination of references fails to teach or fairly suggest a plurality of computer processors, wherein each of said processors is capable of operating as a system management interrupt handler and wherein none of the processors is dedicated to processing system management interrupt of the computer system, are recited in the preamble of independent claim 22. We also conclude that Appellants have not shown that the Examiner erred in combining the teachings of Goodman with other references, in particular, the teachings of Goodman such as utilizing a dedicated processor as the system interrupt handling processor teach away from the claimed invention.

VII. ORDER

We affirm the obviousness rejections of claims 1, 4-8, 16, and 19-23.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

rwk

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